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Implementation of Cognitive Radio Based on SDR and FPGA: Methods, Architectures and Practical Applicability

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Abstract– **This paper explores cognitive radio (CR) technology as a solution to the problem of radio frequency spectrum shortage. The main focus is on the implementation of CR based on a bundle of software-defined radio (SDR) and field-programmable gate arrays (FPGA). The theoretical foundations of CR, key algorithms for dynamic spectrum access (DSA) and parameter adaptation are considered. The role of SDR as a flexible signal processing platform and FPGA as a means of ensuring high performance in real time are analyzed in detail. Practical architectural solutions on popular platforms (USRP, PlutoSDR) and frameworks (GNU Radio, RFNoC) are presented, as well as specific application examples in civil (IoT , 5G/6G) and special areas. Current computational difficulties, energy issues, and prospects for integrating artificial intelligence and neuromorphic computing are discussed**

Keywords— Cognitive Radio, SDR, FPGA, Dynamic Spectrum Access (DSA), Adaptive Systems, Machine Learning, Real-Time Signal Processing.

I. Introduction

The growing demand for wireless communications is confronted with a fundamental limitation: the finite radio spectrum. Traditional static frequency allocations result in inefficient use of frequencies, with large areas ("spectral voids") remaining unoccupied at certain times or locations [1]. Cognitive radio Cognitive Radio (CR), a concept first described in detail by Joseph Mitola in 1999 [2], offers an intelligent approach to solving this problem. CR is a wireless system that can autonomously sense the surrounding electromagnetic environment, analyze the information received, and dynamically adapt its operating parameters (frequency, modulation, power) to optimize communications using unoccupied spectrum without interfering with licensed users (primary users) [3]. Implementation of the complex Sense-Analyze-Adapt cycle requires a unique combination of flexibility and high computing performance, which is provided by the synergy of software-defined radio (SDR) and field-programmable gate array (FPGA) technologies. The objective of this report is to analyze the methods, architectures, and practical applicability of implementing cognitive radio on an SDR+FPGA platform, covering both the theoretical foundations and current technical solutions and development prospects.

II. Purpose and Theoretical Foundations of Cognitive Radio

The main purpose of the CR is to increase the efficiency of spectrum use through dynamic spectrum management (Dynamic Spectrum Access, DSA) [3]. This is achieved by solving key problems:

1. Spectral Void Detection: Identify unoccupied frequency ranges in real time.
2. Adaptation of transmission parameters: Dynamically change the carrier frequency, modulation type (e.g. transition between QPSK, 16-QAM, 64-QAM in OFDM), coding rate, transmission power to maximize throughput or minimize interference and power consumption.
3. Compatibility: Ability to work with multiple existing and future communication standards (Wi-Fi , LTE, 5G, NB-IoT , etc.) within a single hardware platform.
4. Improving reliability and energy efficiency: Ensuring stable communication in conditions of interference (including intentional interference – electronic warfare) and optimizing energy consumption of the radio system.

The theoretical basis of CR is the cognitive cycle [2, 3]:

1. Sensing: Monitoring the radio airwaves to collect data on spectrum occupancy and channel parameters.
2. Analysis / Reasoning: Processing collected data, identifying spectral capabilities, assessing channel quality, predicting the state of the environment, making decisions on necessary adaptations. Machine learning methods are increasingly used here.
3. Action (Adaptation): Adjusting the parameters of the radio transmitter and receiver in accordance with the decision made.
4. Learning (optional): Gaining experience to improve future decisions

III. The role of SDR and FPGA in the implementation of the CR

SDR and FPGA form an ideal technological base for the implementation of computationally intensive and flexible CR:

- SDR (Software-defined radio): Provides a software platform for implementing a wide range of radio signal processing functions (filtering, demodulation, decoding) on general-purpose processors (CPUs) or digital signal processors (DSPs). The key advantage of SDR is reprogrammability, which allows one hardware platform to support multiple communication standards, which is critical for the adaptability of the CR [4]. Popular SDR platforms include USRP (Ettus Research), ADALM-Pluto (Analog Devices) and HackRF.
- FPGA (Field-Programmable Gate Array): Provide high parallel computing performance required for real-time RC operations (especially spectrum sensing tasks). Computationally intensive algorithms (FFT for OFDM, complex filters, correlators for matched filtering, cyclostationarity detectors) can be efficiently implemented on FPGAs as specialized hardware pipelines [5]. FPGAs outperform DSPs in dataflow tasks and offer lower latency than GPUs for deterministic signal processing tasks [6].

IV. Key algorithms and methods for CR on SDR/FPGA

Spectral void detection: Is the most computationally challenging task in the perception cycle.

- Energy Detection (ED): The simplest method that calculates the signal energy in a band. Easily implemented on FPGAs, but is sensitive to threshold and interference [7].
- Matched Filter Detection (MFD): Optimal for detecting known signals (pilot signals), requires precise synchronization and knowledge of the primary user parameters. Implementation on FPGA is efficient [5].
- Cyclostationary Feature Detection (CFD): Detects hidden periodicities (carrier, symbol synchronization) in signals. Provides high accuracy even at low SNR, but requires significant computing resources; for real-time implementation, an efficient FPGA architecture is critical [5, 7].

Adaptive methods:

- Dynamic Frequency Selection (DFS): Switches to a free channel when a primary user is detected or the current channel quality deteriorates.
- Adaptive Modulation and Coding (AMC): Varying the modulation scheme (e.g., from BPSK to 64-QAM) and error correction coding rate depending on the channel signal-to-noise ratio (SNR) to maximize data rate or reliability. OFDM algorithms with adaptive subcarrier allocation fit well into the parallel architecture of FPGAs [8].
- Adaptive Power Control (APC): Minimizes transmit power to reduce interference to other systems and power consumption while maintaining the required link quality (BER).

V. Architectural solutions for CR on SDR/FPGA

The most common and efficient architecture is a hybrid CPU+FPGA [5, 6, 9]:

- CPU (Host Computer): Performs high-level tasks: system management, complex data analysis (including AI/ML algorithms), making strategic decisions about restructuring, interacting with the network, user interface. Runs on an OS (often Linux).
- FPGA: Implements high-performance, low-level, time-deterministic tasks: high-speed DSP (filtering, FFT, detection), RF signal generation/reception (via DAC/ADC), implementation of PHY/MAC layer protocols, data preprocessing for the CPU. Efficient distribution of tasks between the CPU and FPGA is the key to system performance.
- SDR Platforms with FPGA: USRP (with Xilinx family FPGA Spartan or Kintex), ADALM-Pluto (with Xilinx Zynq , which combines an ARM CPU and FPGA), more powerful boards on Zynq Ultrascale+ RFSoC .

Software frameworks :

- GNU Radio: An open source toolkit for building SDR applications. Provides graphical programming of signal processing flows running on the CPU. Can interact with FPGAs via drivers to control the basic functions of the radio frequency board (USRP) [10].
- RFNoC (RF Network on Chip): Framework by Ettus Research, which allows direct development, implementation and control of custom DSP algorithms inside the USRP FPGA boards, integrating them with GNU Radio. Provides much higher performance and flexibility for CR tasks than CPU-only processing [9].

VI. Practical applicability and implementation examples

The advantages of the SDR+FPGA platform for CR (flexibility, performance, adaptability) open up wide application possibilities:

- Civil applications:
  - Wireless Sensor Networks (WSN) and IoT: Devices with CR can find less noisy channels, improving communication reliability and battery life [11].
  - *5G/6G and Future Networks:* CR is a key component for dynamic spectrum sharing (Spectrum Sharing), increasing throughput and reliability in heterogeneous networks (HetNets). SDR/FPGA implementations are used for prototyping and validating new algorithms [8].
  - Smart cities: Adaptive communication systems for infrastructure management, capable of operating in dense radio environments.
- Special applications:
  - Robust communications in EW environments: CR allows communication systems to detect interference and switch to clear frequencies or use

spread spectrum methods that are resistant to suppression [12].
- Adaptive communication systems for UAVs: Drones operating in dynamic environments can use CR to maintain reliable communications with ground control centers and among themselves [11].

- Examples of implementations:
  - Implementation of an Energy Detector (ED) or Cyclostationary Feature Detector (CFD) on USRP N310 FPGA using RFNoC for real-time spectral void detection.
  - Adaptive modulation system based on ADALM-Pluto (Zynq FPGA), changing the modulation scheme (BPSK/QPSK/16-QAM) depending on the measured channel SNR.

5G network prototypes with dynamic spectrum sharing CBRS (Citizens Broadband Radio Service) based on SDR/FPGA platforms.

VII. Difficulties and development prospects

Despite the potential, the implementation of CR on SDR/FPGA faces challenges:
- Computational complexity: Fine detection algorithms (especially CFD) and complex AI-based adaptation require huge FPGA resources.
- Latency: The time spent on the "sense-analyze-adapt" cycle must be minimal for rapid response. Optimization of pipelines on FPGAs is critical.
- Power Consumption: High FPGA performance often comes with increased power consumption, which is problematic for mobile and IoT devices.
- Hidden Node Problem: A situation where a secondary user's transmitter cannot "hear" the primary user's transmitter, but can interfere with it at the receiver.
- Regulation and standardization: Developing a legal framework for dynamic spectrum access.

Promising areas of development:
- Integration with AI/ML: Use of neural networks (including hardware-efficient architectures such as CNN, RNN, Transformer , implemented on FPGAs as neural accelerators) to predict spectrum occupancy, classify signals, and optimize adaptive solutions, which reduces analysis time and improves accuracy [7, 13].
- Neuromorphic and Quantum Computing: Exploring fundamentally new computing paradigms for potential breakthroughs in the speed and energy efficiency of QM signal processing [14].
- Reconfigurable Intelligent Surfaces (RIS): Smart surfaces that re-engineer radio channel characteristics as a complementary technology to CR in 6G networks.
- Development of the hardware base: The emergence of more powerful and energy-efficient FPGAs (e.g., on a 7nm process technology and less) and SoC (System-on-Chip), integrating multi-core CPUs, GPUs and FPGA matrices (like AMD/ Xilinx Versal), will facilitate the implementation of complex cognitive functions.

VIII. Conclusions

Cognitive radio is a revolutionary approach to solving the spectrum shortage problem by turning static radio environment into a dynamic and intelligent one. The implementation of demanding QoS algorithms, especially in real time, is made possible and efficient by the synergy of software-defined radio (SDR) and field-programmable gate array (FPGA) technologies. SDR provides the necessary flexibility and reprogrammability to support multiple standards and adaptive scenarios, while FPGAs provide the computing power and parallelism to implement complex spectrum sensing (DSA) and transmission parameter adaptation algorithms.

Practical implementations on platforms such as USRP, PlutoSDR using GNU Radio and RFNoC frameworks demonstrate the viability of the approach in various domains – from civil applications (IoT , 5G/6G, smart cities) to special systems requiring interference resilience. Despite the existing challenges related to computational complexity, latency and power consumption, the prospects for the development of SDR/FPGA-based CR look extremely promising. The integration of artificial intelligence and machine learning methods implemented directly on FPGAs, as well as the exploration of the potential of neuromorphic and quantum computing, pave the way to the creation of truly intelligent, autonomous and highly efficient wireless communication systems of the future.

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