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FFT IP Cores for HDL from Different Vendors: Comparative Analysis

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***Abstract*— This paper presents a comparative analysis of Fast Fourier Transform (FFT) IP cores for FPGAs from leading manufacturers: AMD (Xilinx), Intel, Microchip and Lattice Semiconductor. The architectures, performance, resource intensity and functionality of the cores when working with fixed and floating points are assessed. Based on the analysis, recommendations are formulated for choosing the optimal solution for tasks of various classes: from high-performance systems (radar, 5G communications) to energy-efficient embedded devices. The report is relevant for DSP engineers and FPGA developers choosing a hardware platform and IP for implementing spectral analysis.**

Keywords*— *Fast Fourier Transform (FFT), FPGA, IP Core, Comparative Analysis, Performance, Resource Intensity, Hardware Implementation

I. Introduction

The Discrete Fourier Transform (DFT) remains the cornerstone of spectral analysis in digital signal processing (DSP), finding applications in radar, communications systems (5G, Wi-Fi), image/audio processing, medical diagnostics and industrial analytics. The high computational requirements of the DFT algorithm ($O(N^2)$) and its optimized version, the Fast Fourier Transform (FFT, O(N log N)) make hardware implementations on Field Programmable Gate Arrays (FPGAs) the preferred solution. FPGAs offer unprecedented parallelism, deterministic performance and energy efficiency. Using ready-made DFT/FFT IP cores from FPGA manufacturers significantly speeds up the development, providing highly optimized and verified solutions tailored to the specifics of the target platform.

The purpose of this paper is to conduct a detailed comparative analysis of DFT/FFT IP cores from leading FPGA manufacturers - AMD (Xilinx), Intel (Altera), Microchip [3] (Microsemi [3]) and Lattice [13] Semiconductor – in terms of architectural features, performance, resource intensity, functionality and practical applicability.

II. Theoretical foundations and motivation

DFT/FFT algorithms: A naive implementation of DFT requires $O(N^2)$ complex multiplication-addition (CMAC), which is unacceptable for large N (1024, 4096, ...). FFT algorithms (Cooley-Tukey [6], etc.) reduce the complexity to O(N log N) by decomposing into basic "butterfly" operations. Key parameters: radix (Radix-2, Radix-4, mixed), method (Decimation-in-Time / Decimation-in-Frequency).

Hardware implementation on FPGA: Main architectures:

- Streaming / Pipelined: High throughput (~1 result/cycle), low latency, high resource intensity. Ideal for stream processing.
- Block (Burst / Buffered): Processes data in blocks. Saves resources by reducing throughput and increasing latency. Suitable for batch processing.
- Massively Parallel: Very high performance but resource intensive, rarely used.

Data Presentation: Critical for accuracy and resources:

- Fixed - Point: Minimal resources (DSP), requires careful scaling to avoid overflow. Up to 34 bits wide (Xilinx).
- Block floating point (Block Floating-Point (BFP): A compromise. Common exponent for a block of data, dynamic range is higher than with fixed point.
- IEEE 754 Floating Point [8]: High precision and dynamic range (Single-Precision - SP, Double-Precision - DP), but significant increase in resources (DSP, memory) and power consumption.

Motivation for using IP cores: Developing a highly optimized FFT from scratch requires deep knowledge of the algorithm and FPGA architecture, is labor-intensive, and error-prone. IP cores:

- Provide ready-made, verified solutions.
- Optimized for specific FPGA resources (DSP blocks, BRAM).
- Have standard interfaces (AXI4-Stream, Avalon-ST) to simplify integration.
- Supported by the manufacturer (updates, new FPGA families).
- Reduces time to market for a product.

III. Detailed analysis of DFT/FFT IP cores by manufacturers

3.1. AMD (Xilinx) - LogiCORE IP Fast Fourier Transform (FFT [1]) v9.1+

Architectures: Wide selection: Pipelined Streaming (max. performance), Radix-4/Radix-2 Burst (resource

saving), Radix-2 Lite (large N), Dynamically Reconfigurable (change N "on the fly").

Data: Fixed-Point (up to 34 bit), Float SP/DP. Flexible format settings.

Size (N): Powers of 2 (8 – 65536+), mixed radixes (2,3,5,7) for Burst .

Interfaces: AXI4-Stream (main), AXI4-Lite (configuration), Native .

Resources/Performance (Kintex example) Ultra Scale+ , N=1024):

- Fixed-Point, Pipelined: ~250-350 DSP, fmax > 300 MHz -> Throughput > 300 MSPS.
- Float SP, Pipelined: ~500-800 DSP, fmax 200-250 MHz -> Throughput ~200-250 MSPS.
- Features: Flexible GUI in Vivado . Scaling, bit-reversal, windowing, real-world signal support, CP (OFDM) insertion/removal. Deep integration with Vivado IPI.

Licensing: Fixed-Point is often included in WebPack. Float SP/DP and advanced versions require a license.

3.2. Intel (Altera) - FFT [2] IP Core

Architectures: Streaming (similar to Pipelined), Variable Streaming (effective for non-powers of 2), Burst.

Data: Fixed-Point , Float SP/DP, BFP.

Size (N): Powers of 2 (8 – 262144+), mixed radix support.

Interfaces: Avalon-ST (main), AMBA AXI4-Stream, Avalon-MM /AXI4-Lite (configuration).

Resources/Performance (example Stratix 10, N=1024):

- Fixed-Point, Streaming: ~200-300 DSP, fmax > 350 MHz -> Throughput > 350 MSPS.
- Float SP, Streaming: ~400-700 DSP, fmax 250-300 MHz -> Throughput ~250-300 MSPS.

Features: Integration with DSP Builder (Simulink). OpenCL support (libraries). Variable mode Streaming for non-standard N. Built-in BFP. Optimization for HyperFlex (Agilex / Stratix 10, fmax > 600 MHz).

Licensing: Fixed-Point is often included in free versions of Quartus . Float and Advanced fixed-point may require a license.

3.3. Microchip (Microsemi [3]) - FPGA DSP: FFT (Libero SoC)

Architectures: Focus on Burst (Radix-2/4) and optimized Streaming / Pipelined for PolarFire . No high-performance Pipelined like Xilinx / Intel .

Data: Fixed-Point , BFP. Float SP is supported to a limited extent. Float DP is rarely supported.

Size (N): Powers of 2 (64 – 8192+). Support for mixed radixes is limited.

Interfaces: Proprietary streaming (similar to Avalon-ST), APB/AXI (configuration).

Resources/Performance (example PolarFire, N=1024, Burst):

- ~50-100 DSP, fmax ~200 MHz. Bandwidth is significantly lower than Pipelined (depends on II).

Features: Optimization for low power consumption PolarFire . Integration with SmartDesign . Emphasis on BFP. Support for SEU mitigation , ECC (PolarFire /RTG4). Integration with RISC-V/ARM cores in SoC FPGA.

Licensing: Often included in Libero SoC (Silver / Gold). Special versions/ Float may require licenses.

3.4. Lattice Semiconductor [13]

Situation: Lack of a universal, highly optimized native Xilinx / Intel level FFT IP core [2].

Alternatives:

- IP from partners (CAST): Commercial Fixed-Point cores. Require separate license. Performance/resources vary.
- *Processor cores (Mico32, RISC-V in Propel):* Software FFT implementations (e.g. CMSIS-DSP). Low performance, small N only.
- Custom RTL implementations: Open (OpenCores [12]) or proprietary. Requires expertise. Efficient for small N (<=64) on iCE40 (Fixed-Point, Radix-2/4).

Focus: Energy-efficient applications with moderate FFT requirements (small N, low sampling rate): sensor processing, simple audio analysis on iCE40UV/ECP5/ CrossLink-NX . Integration with MIPI (CrossLink-NX).

3.5. Third party suppliers (Aldec , CAST, etc.) and Analog Devices [5] (ADI [5])

Third party (eg CAST FFT/IFFT): Cross-platform (VHDL/ Verilog). May offer unique optimizations. Licensing is usually per-use / per-project . Pros: Alternative when native kernels do not match. Cons: Additional cost, more difficult integration, quality of support depends on the vendor .

Analog Devices [5] (AD FFT IP Core): Not a generic core. Part of the reference designs for ADI [5] data acquisition boards (based on Zynq / Intel SoC FPGA). Integrated with Linux drivers , JESD204B/C IP.

Advantages: Quick start with ADI [5] boards.

Disadvantages: Limited customization , tied to ADI [5] ecosystem.

IV. Comparative analysis and practical recommendations

Table 1 – Summary comparison of FFT IP cores

Parameter	AMD (Xilinx)	Intel (Altera)	Microchip (Microsemi)	Lattice Semiconductor
Intended use	HF systems (radar, communications)	RF Systems / Large N	Reliable / Energy efficient / Prom .	Low Power / Sensors
Architectures	Pipeline , Burst (R2/4)	Stream , Var . Stream , Burst	Burst (R2/4)	Burst (R2) / Affiliate
Max. N (effective)	65536+ (Pipeline folded)	262144+ (cascade)	8192	1024 (ECP5/NX), 256 (iCE40)
Data	Fixed , Float SP/DP	Fixed , Float SP/DP, BFP	Fixed , BFP (Float SP rare)	Fixed (12-16 bit)
Pass method.	Very high (Pipeline)	Very high (Stream)	Moderate (Burst)	Low (Burst)
Resources (DSP/LUT)	High (Pipeline)	High (Stream)	Low	Very low / Dependent
Energy consumption	Medium/High	Medium/High	**Low** (PolarFire)	**Extremely low**
fmax (typ.)	500+ MHz (Versal /US+)	600+ MHz (Agilex /S10)	200-250 MHz (PolarFire)	150-200 MHz (ECP5/NX)
Interfaces	AXI4-Stream (standard)	Avalon-ST (standard)	Own / AMBA	Simple / Wishbone
Key Features	Run-time reconfig , Windows, CP	Cascade, Var . Stream ,ATR	SEU Mitigation , BFP	Area, MIPI integrated .
Complexity of integration	Average	Average	Simple	Simple / Dependent
Licensing	Fixed in WebPack , Float is paid	Fixed is often free, Float is paid	Often included, Float is paid	Affiliate / Open Source

V. Recommendations before conclusion

Practical recommendations for selection:

Ultra High Performance / Big N / Floating Point: Choosing Between Xilinx (Versal / Kintex UltraScale+)

and Intel (Agilex / Stratix [10]) . Criteria: ecosystem and specific fmax indicators / resources for the task. Use Pipelined / Streaming architectures.

Performance/resource balance for medium N (up to 16K): Xilinx (Kintex-7/ UltraScale) or Intel (Arria 10) . Choose between Burst (cost savings) and Pipeline (performance) based on throughput requirements.

Reliability / Low power consumption / Strict conditions (Industrial , Space): Microchip [3] (PolarFire / RTG4) . Fixed-Point or BFP . Burst architecture.

Extremely low power consumption / Cost / Small footprint / N up to 1K: Lattice [13] (CrossLink-NX /ECP5) . Fixed-Point. Consider partner IP (CAST) or optimized Open Source implementations for iCE40. Burst architecture.

Systems on a Chip (SoC FPGA): Integration via DMA is Critical. Xilinx Zynq (AXI) , Intel SoC FPGA (Avalon) , Microchip [3] SmartFusion2 (AHB).

Critical aspects when selecting and integrating:

- Requirements: Clearly define N, required throughput (MSPS), latency, precision (data type, bit depth), resource budget (DSP, BRAM, LUT) and power.
- Interfaces: Preference for standards (AXI4-Stream, Avalon-ST) to simplify integration. Consider the need for a configuration interface (AXI-Lite, APB).
- Dynamic reconfiguration: If you need to change N on the fly, only Xilinx fully supports it.
- Documentation and Examples: A Closer Look at User Guides (UG), Product Vendor Guides (PG), timelines and example projects.
- Licensing: Specify inclusion in free versions of software (Vivado WebPack , Quartus Lite) and the cost of licenses for the required functions (especially Float).
- Hidden Complexities: Kernel initialization time, Fixed-Point rounding/scaling peculiarities, bit-reversal delays , memory consumption for coefficients (Twiddle Factors).

VI. Conclusions

The analysis conducted shows that the market for DFT/FFT IP cores for FPGA offers solutions for a wide range of tasks - from extremely high-performance computing to ultra-low-power embedded systems. There is no universal "best" core; the optimal choice is always determined by the specific requirements of the project (N, throughput , latency , accuracy , power , cost , target FPGA).

Key trends:

- Increased use of floating point: Accuracy requirements in modern communication systems (high-level modulations) and radar (anti-jamming), improved Float support in new generation FPGA DSP blocks (Agilex, Versal AI Cores).
- AXI4-Stream Dominance: Standardization Simplifies the Creation of Heterogeneous Systems.
- Optimizing for New Architectures: Active Use of AI Engines at Xilinx Versal and HBM at Intel Agilex for Extreme FFT [2]. Integration of accelerators into RISC-V subsystems (PolarFire SoC).
- Fixed-Point /BFP Role: Critical for applications where resources and power consumption are limited and dynamic range is manageable.
- Development of Open Source alternatives: For small N and budget designs (especially on the Lattice [13] iCE40) optimized RTL implementations remain a viable option.

Recommendations for further work:

- Specific modeling: For the final selection, perform synthesis and analysis of time characteristics (Static Timing Analysis) of selected IP cores on a specific target FPGA and for specific parameters (N, data type, architecture).
- Power Analysis: Use Power Estimation Tools (Vivado Power Estimator, Quartus PowerPlay) for selected configurations.
- Integration testing: Develop a test environment (Testbench) to check the interaction of the BPF IP core with other system components (ADC/DAC, processor, memory) through selected interfaces.
- Exploring Hybrid Approaches: Evaluating the Use of RISC-V Vector Extensions in Combination with Hardware Accelerators or Small FPGAs for Specific Spectral Analysis Tasks.

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