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Orthogonal Sequence Utilization in Digital System Design

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***Abstract*— Code division multiple access (CDMA) is one of the fundamental multiple access methods used in digital communication systems. This essay examines the architecture of CDMA, principles of constructing orthogonal codes, modeling CDMA in Octave and Python environments , and the basics of implementing a CDMA module in FPGA using the VHDL hardware description language. The goal of the work is to prepare for the creation of a prototype of the digital part of the device based on STM32 or FPGA.**

Keywords*— CDMA, Orthogonal Codes, Walsh Codes, Gold Codes, Octave Simulation, VHDL Implementation, FPGA, Correlator.

I. Introduction

Code Division Multiple Access (CDMA) is a multiple access method that allows multiple transmitters to simultaneously use a common frequency band by using unique orthogonal or quasi-orthogonal codes. Due to the minimization of mutual interference, CDMA is widely used in mobile communications, GPS and wireless sensor networks [1, 2]. The purpose of this paper is to study the CDMA architecture, simulate its operation in software environments, and develop a hardware implementation for subsequent prototyping on STM32 or FPGA. The relevance of the study is due to the growing requirements for noise immunity and throughput of wireless systems.

II. Types of codes and properties of sequences

Orthogonal codes

• Walsh codes: Are constructed based on Hadamard matrices of order $N=2^k$. Have strict orthogonality:

$$\sum_{i=0}^{N-1} W_n(i) \cdot W_m(i) = 0 \quad (n \neq m).$$

where W_n, W_m are different code sequences [2]. Advantages: simplicity of generation, ideal separability in synchronous systems. Limitation: effective only with full synchronization.

• Gold codes: Are formed as G = A xor B cdot D, where A,B are M-sequences, D is a shift mask.

Possess:

o Low level of cross-correlation ($R_{xy}(\tau)$ ≤sqrt{2^(n+1)})

o Large family of codes (N+2 sequences for length 2^{n-1}) [4].

o Used in asynchronous systems (GPS, CDMA2000).

Quasi-orthogonal sequences

• Kasami codes: A subset of Gold codes with minimal cross-correlation R_{max} = sqrt(N+1).

Feature: compact hardware implementation due to recursive structure [3].

• M-sequences: Linear LFSR sequences with autocorrelation peak $R_{xx}(0)=1$, $R_{xx}(\tau \neq 0) \approx -1/N$. Used as a basis for complex codes [1].

Table 1 – Comparative characteristics

Parameter	Walsh	Gold	Kasami
Orthogonality	Full	Partial	Partial
Number of codes	N	N+2	Sqrt(N)
Correlation (in symbols)	0 (sync.)	≤65	≤1$
Application	Downlink	GPS/GNSS	Sensor nets

CDMA is based on the generation of orthogonal codes that ensure channel separation. Walsh codes are constructed on the basis of Hadamard matrices, which have the property of pairwise orthogonality of rows. An alternative is Gold codes , formed by a combination of two maximal linear sequences, which increases resistance to interference [3].

At the transmission stage, the user data is multiplied by its unique code. The receiver extracts the target signal by correlating the mixed input signal with the reference code. The key requirement is minimal cross-correlation between the codes of different users, which reduces interference [4].

III. CDMA system architecture

CDMA modeling in Octave includes Hadamard matrix generation, signal superposition, and correlation analysis. An example implementation of the Hadamard matrix generation function:

```
function H = hadamard_matrix ( n )
  if n == 1
H = 1 ;
  else
```

```
Hn_1 = hadamard_matrix ( n / 2 );
H = [ Hn_1 , Hn_1 ; Hn_1 , - Hn_1 ];
  endif
endfunction
```

In Python, similar tasks are solved using the NumPy and SciPy libraries. The Walsh code generation function demonstrates the conciseness of the language:

```
import numpy as np
def hadamard_matrix ( order ):
  if order == 1 :
    return np . array ([[ 1 ]])
  else :
H_n1 = hadamard_matrix ( order // 2 )
    return np . block ([[ H_n1 , H_n1 ],
 [ H_n1 , - H_n1 ]])
```

Both tools confirmed the effectiveness of orthogonal codes for signal separation.

IV. Implementation on FPGA using VHDL

Implementation plan:

- Generating codes in hardware.
- Hardware correlation of received signals.
- Implementation of filtering and selection of useful signal.

Structural components of the project:

- Code generation module.
- Modulation module (multiplication of data by code).
- Demodulation module (correlation).
- Control interface (e.g. via AXI or UART).

The hardware implementation of CDMA on FPGA includes three key modules:

Code Generator - Creates Walsh / Gold sequences .

Modulator - multiplies data by user code.

Correlator - isolates a signal from a mixture.

Example of VHDL description of a correlator:

```
library ieee ;
use ieee . std_logic_1164 . all ;
use ieee . numeric_std . all ;

entity correlator is
  port (
    clk , reset : in std_logic ;
    input_signal : in std_logic_vector (
 7 downto 0 );
    code_sequence : in std_logic_vector
( 7 downto 0 );
    correlation_out : out signed ( 15 do
wnto 0 )
  );
end entity ;

architecture Behavioural of correlator i
s
begin
  process ( clk , reset )
  begin
    if reset = '1' then
      correlation_out <= ( others => '0'
 );
    elsif rising_edge ( clk ) then
      correlation_out <= correlation_out
 +
        ( signed ( input_signal ) * sign
ed ( code_sequence ));
    end if ;
  end process ;
end architecture ;
```

An interface (AXI or UART) is used to control the modules. The advantage of FPGA is parallel processing, which is critical for high-speed systems [5].

V. Conclusions

The study confirmed the efficiency of CDMA for multiple access systems. Modeling in Octave and Python allowed us to analyze the properties of orthogonal codes, and the implementation of basic modules in VHDL created a basis for prototyping on FPGA. The STM32 microcontroller is suitable for control and interface logic, while the FPGA will provide high-speed signal processing. A promising direction is the development of adaptive systems with dynamic code generation. Critical success factors: code synchronization and minimization of delays in correlators.

References

[1] Proakis JG *Digital Communications* /JG Proakis . - 5th ed . — New York : McGraw-Hill , 2007. - 1150 p .

[2] Haykin S. *Communication Systems* / S. Haykin . - 5th ed . - Hoboken : Wiley , 2009. - 816 p .

[3] Rappaport TS *Wireless Communications : Principles and Practice* /TS Rappaport . —Upper Saddle River : Prentice Hall , 2002. — 707 p .

[4] Sklar B. *Digital Communications : Fundamentals and Applications* /B. Sklar . - 2nd ed . —Upper Saddle River : Prentice Hall , 2001. — 1079 p .

[5] IEEE Standard VHDL Language Reference Manual (IEEE Std 1076-2019). - IEEE, 2019.

[6] Octave Documentation [Electronic resource]. — URL: https://docs.octave.org (date of access: 30.07.2025).

[7] NumPy Documentation [Electronic resource]. — URL: https://numpy.org/doc (date of access: 30.07.2025).

[8] Orthogonal Codes Overview [Electronic resource] // Wikipedia . — URL: https://en.wikipedia.org/wiki/Orthogonal_code (date of access: 30.07.2025).