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Research of Complexity Characteristics of Synchronized Accumulative Adders

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***Abstract*— The scope of application of single-bit and multibit accumulative adders in processors and coprocessors of arithmetic and logic devices of computers is substantiated. The structures of synchronized accumulative adders with high performance and minimal hardware complexity are proposed. The system characteristics of speed, hardware and structural complexity of synchronized accumulative adders are calculated. A method for improving the performance of this class of accumulative adders is proposed.**

Keywords*— *Accumulative Adder, Performance, ALU, Algorithm, Operation, Hardware Complexity, Time Complexity

I. Introduction

Digital processing of binary-coded data in computer technology is realized by microelectronic structures that perform computational operations such as multiplexing, comparison, addition/subtraction, squaring/multiplication, division and square root extraction, and others in arithmetic-logical units (ALUs) of processors [1-5].

Methods for implementing mathematical operations in arithmetic and logic devices of computer processors are chosen taking into account the required speed, type of number representation, number system, and other technical, economic, and system factors. The criterion for choosing a particular method is usually to achieve the minimum price, maximum performance, or the optimal ratio of performance and price [1,7].

The operation of adding binary numbers [9-10] is the most commonly used in many computer applications among other operations, and an important task is to develop high-speed devices for summing multi-bit binary numbers.

The analysis of classes of structures and microelectronic implementations of components of ALP coprocessors of modern computers shows that unsynchronized combinational adders (UCA) and computing structures based on them are exclusively used as their components [11,12].

As a result of the use of classical binary arithmetic and multibit structures of combinational adders with through transfers, a modern problem of developing theoretical provisions and corresponding microelectronic means of performing arithmetic operations with increased by 1-2 orders of magnitude the speed of arithmetic computation was formed [13,14].

Therefore, an important task is to develop methods for expanding the functionality and increasing the speed of synchronized accumulative adders used as components in multipliers, quadrats, and other devices for performing arithmetic operations [15-18].

II. Structure and System Characteristics Synchronized Accumulative Adders

In work [16], the system characteristics of the structural, time, and hardware complexity of single-bit and multibit combinational binary adders were studied and presented. An analysis of the classes of structures and microelectronic implementations of the components of the ALU coprocessors of modern computers shows that unsynchronized combinational adders and computing structures based on them are exclusively used as their components [15,16]. The use of this class of adders in powerful vector and scalar supercomputers that implement deeply parallelized computing processes and accumulate large data arrays requires high-performance synchronization, which can be ensured by using synchronized single-bit and multibit accumulative adders in their architectures.

An example of the implementation of this class of adders is the architecture of a synchronized accumulative adder (SAA), which is shown in Fig. 1.

The structure of the full single-bit synchronized adder includes: 1,2 - the corresponding information inputs ai and bi; 3,4 - the first and second logical elements “Exclusive AND”, respectively; 5 - sum output Si; 6 - the third input of the carry adder C_{in}; 7,8 - the first and second logical elements AND-NOT; 9 - D-trigger; 10 - write

synchronization input S_x; 11,12 - the corresponding, direct C_{out} and inverted not C_{out} second and third outputs of the carry adders C_{out} and not C_{out} [19].

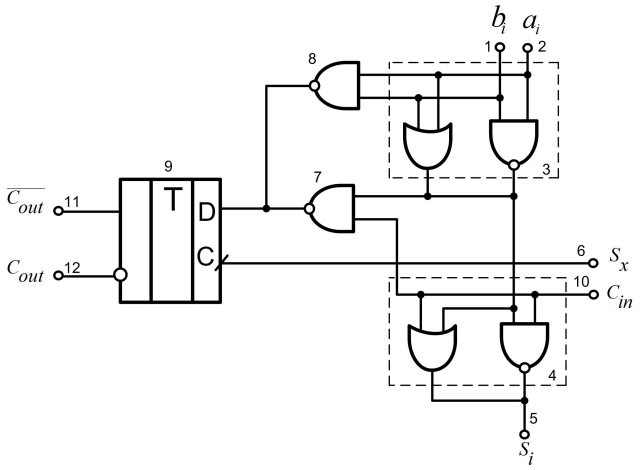


Fig. 1. The structure of full single-bit synchronized adder

A full single-bit synchronized adder operates as follows: when bits of logical units 1 or 0 are applied to the adder information inputs a_i (1) and b_i (2), the output of the first logic element "Exclusive AND" (3) generates the corresponding signals of their logical processing: "1" if the inputs ai and bi are the combination "01" or "10" and "0" if the inputs ai and bi are the combination '00' or "11". The resulting bit "0" or "1" at the output of the first logical element "Exclusive AND" (4) is fed to the first input of the second logical element "Exclusive AND", the second input of which receives the bit '0' or "1" of the input end-to-end carry C_{in} (10). At the output (5) of the second logical element "Exclusive AND", the bit '0' or "1" of the sum of the input signals of the adder S_i (5) is similarly formed.

At the same time, when the signals '0' or '1' are applied to the inputs of the adder a_i (1), b_i (2) and the input carry signal C_{in} (6), which are applied to the corresponding inputs of the logical elements "AND-NOT" (7 and 8), the inverted bit of the output carry (not C_{out}) is formed at their combined outputs, which is written to the trigger (9) by the rising edge of the synchronization signal S_x applied to the C-input of the D-trigger, at the direct and inverted outputs of which the parallel signal C_{out} (11) and not C_{out} (12) of the output end-to-end carry of the full single-bit synchronous adder is formed.

The proposed full single-bit synchronized adder is characterized by reduced hardware complexity, compared to the known combinational adders without memory, contains 6 logic gates and one D-trigger in the path of end-to-end transfer to the high bit. Compared to the known memoryless combinational adders [21], which contains 11 gates, the proposed adder is characterized by reduced hardware complexity. This was achieved by using a D-trigger in the end-to-end transfer path, which made it possible to use a 6-gate full combinational adder with an inverted end-to-end transfer output, which is inverted at the inverted output of the trigger into a direct output (C_{out}).

It should be noted that when using in multi-bit binary adders built on the basis of SAA input/output series-connected C_{in} -> C_{out} transfers, the signal delay is 2n-microcycles. When used in multi-bit binary adders (MBA), the signal delay in the C_{in} -> C_{out} path is 3 microcycles regardless of the bit depth, since the propagation of end-to-end transfers is absent in each microcycle of adding two n-bit binary codes.

The achieved expansion of the functionality of a complete unsynchronized single-bit adder by introducing a memory element based on a synchronized D-trigger into its structure made it possible to synchronize the operation of computing structures based on the use of such adders with a clock frequency of performing operations of adding multi-bit numbers with a delay of 4 microcycles, regardless of the bit depth of the computing structures.

The parallel generation of parallel-phase through-carry signals C_{out} and not C_{out} at the outputs of the D-trigger extends the possibilities of joint use of the proposed full single-bit adder in computing structures with direct and inverted horizontal through-carry inputs, including with extremely minimal delays of the signals of sum formation and transfers by 1 microcycle.

The disadvantage of such an SAA1 (Fig. 1) is the limited functionality due to the fact that such a complete single-bit synchronized binary adder does not contain a second memorizing D-trigger at the output of the second logical element "Exclusive AND" [19]. Another disadvantage of such an adder is the lack of information connection between the output of the second logical element "Exclusive AND" and the input of the first logical element "Exclusive AND", as well as the lack of an information input (R_0) connected to the R-input of the D-trigger.

In work [20], the structure of an improved SAA2 with extended functionality is proposed. This SAA2 is used as a Guild sell in the structures of matrix multipliers by Brown, Dudd, Wallace, and others [7-10]. The architecture of such an SAA2 is shown in Fig. 2.

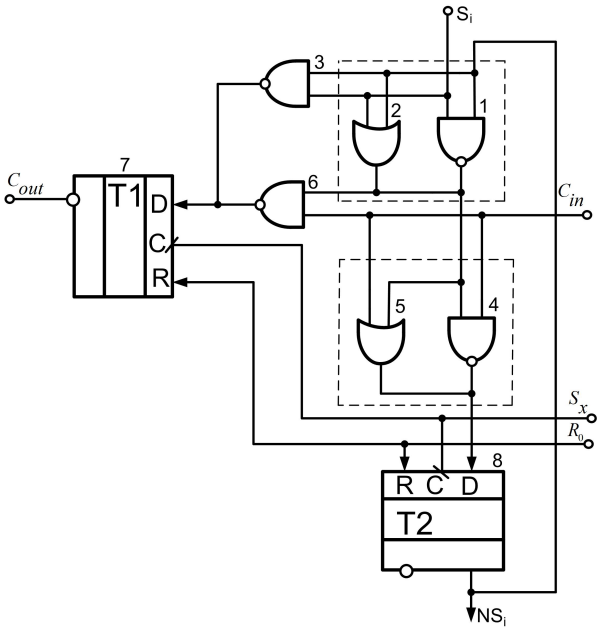


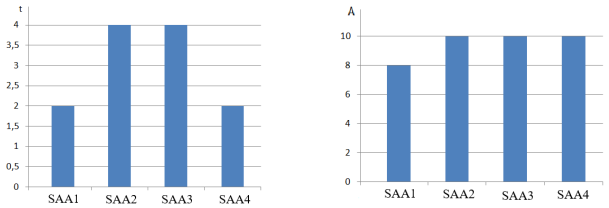
Fig. 2. The structure of an advanced full single-bit adder

The disadvantage of such an SAA2 is its limited functionality due to the fact that its structure does not contain a complete single-bit adder and a carry input (C_{in}) as a component of a multi-bit SNS. Another disadvantage of this adder is its low speed, which is due to the presence of a feedback of the direct output of the second D-trigger of the sum bit accumulation Si with the second input of the incomplete single-bit adder.

Increasing the performance of the improved SAA2 by 2 times compared to the known architecture (SAA1) is achieved by the presence of an information link between the output of the full combinational adder and the second information input. At the same time, the delay of signals with a duration of 2 microcycles in the full combinational adder is synchronized with the delay of signals with a duration of 2 microcycles in the D-trigger of the end-to-end transfer.

The hardware complexity of the studied SNS is calculated according to the expression: $A= A_1+ A_2 +A_3$, where A_1-A_3 are the hardware complexities of the corresponding components of the SAA, A_1=3 gates (single-bit half adder); A_2 =6 gates (single-bit full adder); A_3=2 gates (D-trigger).

In Fig. 3 shows the characteristics of the time and hardware complexity of the studied architectures of single-bit SAA.



a) b)

Fig. 3. Characteristics of time (a) and hardware complexity (b) of the studied SAA

III. Conclusions

The paper substantiates the scope of application of single-bit and multibit accumulative adders in processors and coprocessors of arithmetic and logic devices of computers. The structures of synchronized accumulative adders with high performance and minimal hardware complexity are proposed. The system characteristics of speed and hardware complexity of synchronized accumulative adders are calculated. A method for improving the performance of this class of accumulative adders is proposed. Increasing the performance of the improved accumulative synchronized adder is achieved through structural improvements.

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