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Transforming IC Design with Agent-Based Artificial Intelligence

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***Abstract*— The Cadence Voltus InsightAI design system integrates generative AI technology to address voltage drop issues early in the design process and automatically improve designs, providing rapid, automated reduction of supply voltage drop, increased productivity, and improved power, performance, and area performance. Voltus InsightAI integrates with Cadence's complete digital workflow to provide design corrections that are time- and rule-based.**

Keywords*— PPA, TAT, EDA, DRC, PDN, EM-IR, Power integrity, IR-Driven Design.

I. Introduction

At advanced nodes, there is a deep conflict between power, performance, area (PPA), and design turnaround time (TAT). New physical and electrical design challenges arise, and structures such as FinFETs create new needs.

The increasing penetration of artificial intelligence (AI) functions in many industries is leading to a significant increase in the complexity of integrated circuit design and architecture. Also, when you combine the design complexity with the ever-increasing requirements for power consumption, performance, and area, integrated circuit designers are now faced with increasing demands to develop smaller, faster, and more economical devices in ever-more productive devices [1].

II. Challenges in power integrity and electromagnetic compatibility

One of the challenges in this direction is power integrity and electromagnetic compatibility. In complex designs, designers regularly encounter many EM-IR violations during the formation of connections, making it imperative to address this problem early in the design process.

However, one of the main bottlenecks in the electromagnetic analysis of a design is that it is very computationally complex and costly due to the size and interconnected nature of the power system.

This violation is the principal contradiction. To address these design challenges, as devices built to support increasingly complex and demanding features, especially AI, AI needs to be built early in the design process.

Cadence is taking this approach with Voltus InsightAI, the industry's first generative AI technology that automatically identifies the root cause of compatibility violations early in the design process and selects and implements the most effective methods to improve performance and density. With Voltus InsightAI, developers can fix up to 95% of design rule violations, resulting in a 2X increase in productivity [2].

Voltus InsightAI is the industry's first EDA product that uses AI to effectively predict root causes and resolve signal and power integrity issues at the design implementation stage and is fully compatible with Cadence's full-stack workflow to provide design corrections that take into account timing and design rules (DRC). Voltus InsightAI integrated with Cadence's Innovus implementation system, which enables designers to reduce power consumption significantly, latency, improve signal and power integrity, prevent short circuits, and achieve potential density/quality benefits, effectively reducing today's congested power distribution networks (PDN). One of the significant challenges is power integrity, which is becoming more challenging in advanced technology nodes as designers place more transistors in smaller and denser spaces. This results in a significant increase in power density, especially for 5nm and below. Previously, there might only be hundreds or thousands of IR (resistive power loss) disturbances in a design and interface, so these issues could be addressed manually. However, other mechanisms are needed for large designs with high element density. Using Voltus InsightAI, designers can use internal design analysis to improve power integrity on the die or the chiplets [3].

Power integrity and PDN analysis

Power integrity affects many aspects of integrated circuit performance, and ensuring power integrity in digital design begins with ensuring that the power network impedance is as low as possible. To minimize voltage spikes that can cause circuit elements to malfunction, some basic design steps are used to help achieve the desired result. PDN analysis is performed in two modes: time domain and frequency domain. If sufficiently accurate models for PDN impedance are built, it is possible to compare the transients in the network with the power fluctuation limits in the system. PDN analysis is also performed in the frequency domain, allowing us to determine a digital or analog system's signal bandwidths and power levels. Power network design aims to ensure that DC and/or AC power is delivered to the appropriate units. High-speed digital and analog systems have both components in some system areas, so power integrity must be considered on both sides.

In DC systems with resistive components, power delivery is a relatively simple concept; power is dissipated in the load depending on the load resistance. Therefore, DC PDN analysis considers only the resistive power losses in all conductors leading to the respective loads. This requires calculating the current density in the power planes and rails used to distribute the power, which can be visualized as a color map of the crystal topology.

AC analysis is more complex and has a noise problem. With TTL technology operating at high core voltages, many power integrity issues could be ignored because the noise margins in the logic circuits of these components were huge. Today's components typically operate at core voltages of 1.8...3.3V with less noise margin and many inputs/outputs.

Therefore, the impedance of the power rails will affect the following characteristics of the integrated circuits:

• Power rail noise. PDN voltage ripples are created by transient currents that interact with high reactive impedance at specific frequencies;

• Power line noise damping. The amount of resistance and losses in the substrate will manifest as ringing (i.e., oscillations that are not sufficiently damped);

• Reverse current will follow the path of least resistance (for DC) or least reactance (for AC). It is necessary to ensure minimum inductance and maximum capacitance of the planes throughout the PDN;

• Signal jitter. A signal jitter is caused by a surge of transient current that propagates to the inputs/outputs, which interferes with the operation of the logic. These problems can be reduced by using different plane layers for power routing, placing power and ground traces next to each other, and using multiple planes in parallel.

Innovus Key Features and Benefits:

• Massively parallel architectures to handle large projects and support multi-threading on multi-core workstations, as well as distributed processing over computer networks;

• New placement technology based on the GigaPlace solver, which takes into account latency and topology, pin access provides optimal element and trace placement, performance, and PPA;

• Advanced multi-threaded layer-aware optimization engine, which is time and power-driven to reduce dynamic power and energy leakage;

• Parallel clock and data path optimization engine for better inter-loop variability and performance with reduced power consumption;

• Next-generation Slack-driven (Slack – operating system for work) routing with track-aware time optimization that considers signal integrity at an early stage and improves post-routing correlation;

• Full-flow multi-objective technology to support simultaneous electrical and physical optimization;

• Customizable process through a common interface for the developer and team for synthesis, implementation, and sign-off with reliable reporting and visualization, contributing to design efficiency and productivity.

The Innovus placement system features a new GigaPlace engine that changes the way placement is done and improves PPA. The GigaPlace engine is time-driven and tightly integrated. With this approach, the engine helps place cells in a time-driven manner by creating a profile of path time constraints and making placement adjustments based on these time constraints [4].

Early Prediction of IR Problems and IR-Driven Design Improvement

The deployment system shares a common user interface with Cadence's Genus Synthesis Solution and Tempus Timing Signoff Solution. The system simplifies command naming and aligns common deployment methods across these Cadence digital and signing tools. For example, project initialization, database access, command consistency, and metrics collection processes have been streamlined and simplified. In addition, updated and standard methods were added for starting, defining, and deploying link flows. These updated interfaces and link flows improve productivity by providing a familiar interface across the core deployment and signing products.

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